ABSTRACT

0030 A gate structure and method for forming the same the method including providing a silicon substrate including one of N and P-well doped regions and an overlying the CVD silicon oxide layer; forming an opening in the CVD silicon oxide layer to include a recessed area extending into a thickness portion of the silicon substrate; thermally growing a gate oxide over exposed silicon substrate portions of the recessed area; backfilling the opening with polysilicon; planarizing the polysilicon to the opening level to reveal the silicon oxide layer; and, selectively removing the silicon oxide layer to form a recessed gate structure.